**WESTERN DIGITAL**
CORPORATION

# WD279X-02 Floppy Disk Formatter/Controller Family

## FEATURES

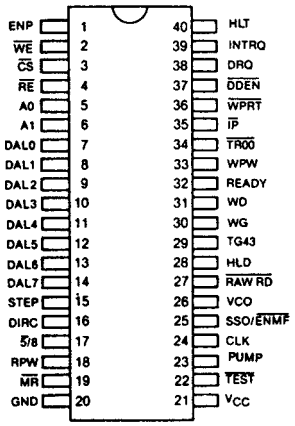
- ON-CHIP PLL DATA SEPARATOR
- ON-CHIP WRITE PRECOMPENSATION LOGIC
- SINGLE +5V SUPPLY
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 (FM)
  - IBM 34 (MFM)
- AUTOMATIC SEEK WITH VERIFY
- MULTILE SECTOR READ/WRITE
- TTL COMPATIBLE
- PROGRAMMABLE CONTROL
  - SELECTABLE TRACK-TO-TRACK ACCESS
  - HEAD LOAD TIMING
- SOFTWARE COMPATIBLE WITH THE FD179X SERIES
- SOFT SECTOR FORMAT COMPATIBILITY

## DESCRIPTION

The WD279X are N-Channel Silicon Gate MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The WD279X, which can be considered the end result of both the FD1771 and FD179X designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD279X contains all the features of its predecessor the FD179X plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD179X and WD279X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical.

Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

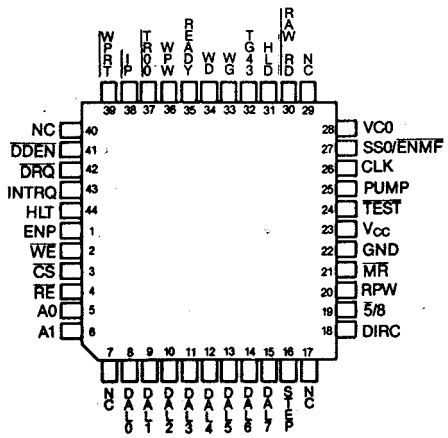
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The WD279X is set up to operate on a multiplexed bus with other bus-oriented devices.




PIN DESIGNATION

The WD279X is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The WD2793 is identical to the WD2791 except the DAL lines are TRUE for systems that utilize true data busses.

The WD2795/7 has a side select output for controlling double-sided drives.



**PIN DESCRIPTION**

| PIN NUMBER | SIGNAL NAME | MNEMONIC | FUNCTION |
|---|---|---|---|
| 1 | ENABLE PRECOMP | ENP | A Logic high on this input enables write precompensation to be performed on double density Write Data output only. |
| 19 | MASTER RESET | $\overline{MR}$ | A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register. |
| 20 | POWER SUPPLIES | $V_{SS}$ | Ground |
| 21 | | $V_{CC}$ | +5V ±5% |
| **COMPUTER INTERFACE:** | | | |
| 2 | WRITE ENABLE | $\overline{WE}$ | A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low. |
| 3 | CHIP SELECT | $\overline{CS}$ | A logic low on this input selects the chip and enables computer communication with the device. |
| 4 | READ ENABLE | $\overline{RE}$ | A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low. |
| 5,6 | REGISTER SELECT LINES | A0,A1 | These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:<br>$\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$<br>0 0 0 Status Reg Command Reg<br>0 0 1 Track Reg Track Reg<br>0 1 0 Sector Reg Sector Reg<br>0 1 1 Data Reg Data Reg |
| 7-14 | DATA ACCESS LINES | DAL0-DAL7 | Eight bit bi-directional bus used for transfer of commands, status, and data. These lines are inverted (active low) on WD2791 and WD2795. |
| 24 | CLOCK | CLK | This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for mini-floppies. |
| 38 | DATA REQUEST | DRQ | This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR. |

**PIN DESCRIPTION (Continued)**

| PIN NUMBER | SIGNAL NAME | MNEMONIC | FUNCTION |
|---|---|---|---|
| 39 | INTERRUPT REQUEST | INTRQ | This output is set at the completion of any command and is reset when the Status register is read or the command register is written to. |
| **FLOPPY DISK INTERFACE:** | | | |
| 15 | STEP | STEP | The step output contains a pulse for each step. |
| 16 | DIRECTION | DIRC | Direction Output is active high when stepping in, active low when stepping out. |
| 17 | 5 1/4," 8" SELECT | $\overline{5/8}$ | This input selects the internal VCO frequency for use with 5 1/4" drives or 8" drives. |
| 18 | READ PULSE WIDTH | RPW | An external potentiometer tied to this input controls the phase comparator within the data separator. |
| 22 | $\overline{\text{TEST}}$ | $\overline{\text{TEST}}$ | A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins. |
| 23 | PUMP | PUMP | High-Impedance output signal which is forced high or low to increase or decrease the VCO frequency. |
| 25 | $\overline{\text{ENABLE MINI-FLOPPY}}$ (2791, 2793) | $\overline{\text{ENMF}}$ | A logic low on this input enables an internal ÷2 of the Master Clock. This allows both 5 1/4" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a Logic 1. |
| 25 | SIDE SELECT OUTPUT (2795, 2797) | SSO | The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector ID Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition. |
| 26 | VOLTAGE-CONTROLLED OSCILLATOR | VCO | An external capacitor tied to this pin adjusts the VCO center frequency. |
| 27 | $\overline{\text{RAW READ}}$ | $\overline{\text{RAW READ}}$ | The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition. |
| 28 | HEAD LOAD | HLD | The HLD output controls the loading of the Read-Write head against the media. |
| 29 | TRACK GREATER THAN 43 | TG43 | This output informs the drive that the Read/Write head is positioned between track 44 and the inside track. This output is valid only during Read and Write Commands. |

**PIN DESCRIPTION (Continued)**

| PIN NUMBER | SIGNAL NAME | MNEMONIC | FUNCTION |
|---|---|---|---|
| 30 | WRITE GATE | WG | This output is made valid before writing is to be performed on the diskette. |
| 31 | WRITE DATA | WD | MFM or FM output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats. |
| 32 | READY | READY | This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7. |
| 33 | WRITE PRECOMP WIDTH | WPW | An external potentiometer tied to this input controls the amount of delay in Write precompensation mode. |
| 34 | $\overline{\text{TRACK 00}}$ | $\overline{\text{TR00}}$ | This input informs the WD279X that the Read/Write head is positioned over Track 00. |
| 35 | $\overline{\text{INDEX PULSE}}$ | $\overline{\text{IP}}$ | This input informs the WD279X when the index hole is encountered on the diskette. |
| 36 | $\overline{\text{WRITE PROTECT}}$ | $\overline{\text{WPRT}}$ | This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit. |
| 37 | $\overline{\text{DOUBLE DENSITY}}$ | $\overline{\text{DDEN}}$ | This input pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. |
| 40 | HEAD LOAD TIMING | HLT | When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD. |

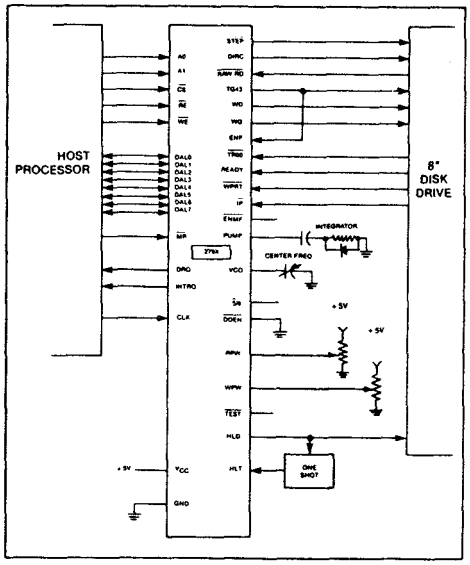



**Figure 1.**

## APPLICATIONS

8" FLOPPY AND 5 1/4" MINI-FLOPPY CONTROLLER SINGLE OR DOUBLE DENSITY CONTROLLER/-FORMATTER

The WD279X Family are MOS/LSI devices which perform the functions of a Floppy Disk Controller/Formatter. Software compatible with its predecessor, the FD179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.

When operating in Double Density mode, Write Precompensation may be enabled, its value predetermined by an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5 1/4" or 8" Floppy Disk interfacing.

The WD279X is fabricated in NMOS silicon gate technology and available in a 40-pin dual-in-line package, as well as 44-pin quad packs.

| FEATURES | 2791 | 2793 | 2795 | 2797 |
|---|---|---|---|---|
| Single Density (FM) | X | X | X | X |
| Double Density (MFM) | X | X | X | X |
| True Data Bus | | X | | X |
| Inverted Data Bus | X | | X | |
| Side Select Out | | | X | X |
| Internal CLK Divide | X | X | | |

## ORGANIZATION

Refer to the Floppy Disk Formatter block diagram in Figure 2. The primary sections include the parallel processor interface and the Floppy Disk Interface.

**Data Shift Register** - This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register** - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Track Register** - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

**Sector Register (SR)** - This 8-bit register holds the address of the sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)** - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)** - This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

**CRC Logic** - This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)** - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control** - All computer and Floppy Disk interface controls are generated through this logic.

The internal device timing is generated from an external crystal clock.

**AM Detector** - The address mark detector detects ID, data and Index address marks during read and write operations.

**Write Precompensation** - enables write precompensation to be performed on the Write Data ouput.

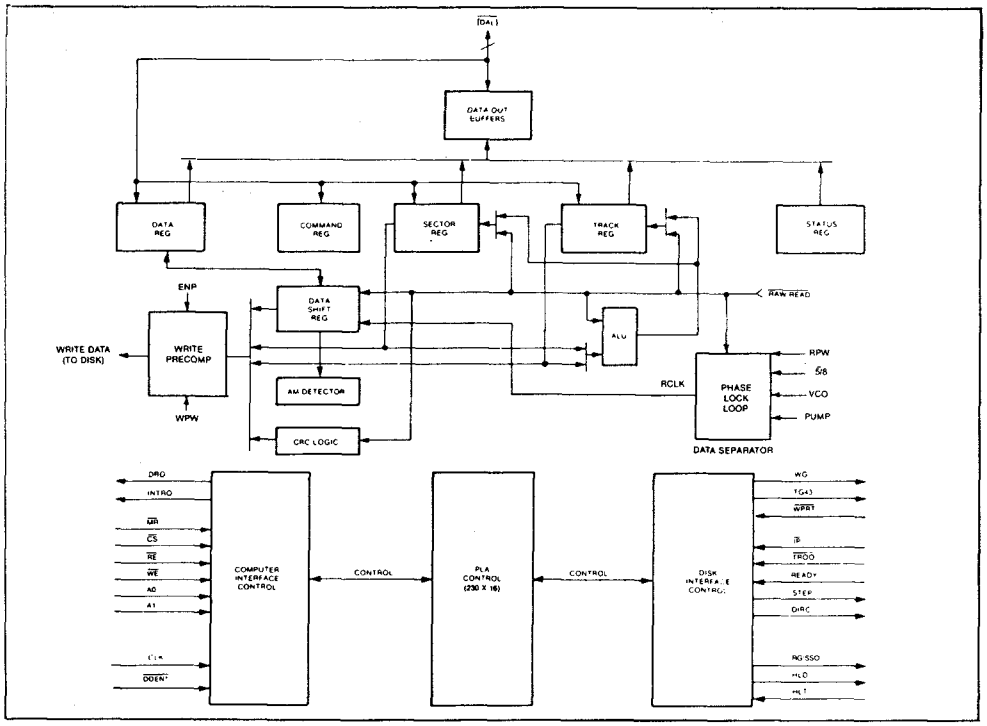



**Figure 2. WD279X BLOCK DIAGRAM**

**Data Separator** - a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼" or 8" Floppy Disk interfacing.

**PROCESSOR INTERFACE**

The Interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD279X. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

| A1 | A0 | READ ($\overline{RE}$) | WRITE ($\overline{WE}$) |
|---|---|---|---|
| 0 | 0 | Status Regiser | Command Register |
| 0 | 1 | Track Register | Track Register |
| 1 | 0 | Sector Register | Sector Register |
| 1 | 1 | Data Register | Data Register |

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD279X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD279X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for 5 1/4" drives.

On the WD2791/WD2793, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both 5 1/4" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal ÷2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both 5 1/4" and 8" configurations.

The internal VCO frequency must also be set to the proper value. The $\overline{5/8}$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5/8}$ = 0, 5 1/4" data separation is selected; when $\overline{5/8}$ = 1, 8" drive data separation is selected.

| CLOCK (24) | $\overline{ENMF}$ (25) | $\overline{5/8}$ (17) | DRIVE |
|---|---|---|---|
| 2 MHz | 1 | 1 | 8" |
| 2 MHz | 0 | 0 | 5¼ |
| 1 MHz | 1 | 0 | 5¼ |

**FUNCTIONAL DESCRIPTION**

The WD279X-02 is software compatible with the FD179X-02 series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 179X can be transferred to a 279X system without modification.

In addition to the WD179X, the WD279X contains an internal Data Separator and Write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished.

A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate Write Data pulse widths.

Similarly, Data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5 MHz for 8" drives). The VCO Trimming capacitor (Pin 26) is adjusted for center frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the WD179X.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, $\overline{TEST}$, and $\overline{MR}$.

**GENERAL DISK READ OPERATIONS**

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0". Sector lengths are determined at format time by the fourth byte in the "ID" field.

| Sector Length Table* | |
|---|---|
| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |

*2795/97 may vary - see command summary.

The WD279X recognizes tracks and sectors numbered 00-FF Hex. However, due to programming restrictions, only tracks and sectors 00 through F4 can be formatted.

**GENERAL DISK WRITE OPERATION**

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater then the precomp adjustment. Write Data provides the unique address marks in both formats.

**READY**

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low, the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

**COMMAND DESCRIPTION**

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**TABLE 1. COMMAND SUMMARY**

A. Commands for Models: WD2791, WD2793 — B. Commands for Models: WD2795, WD2797

| Type | Command | Bits 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bits 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I | Restore | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| I | Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| I | Step | 0 | 0 | 1 | T | h | V | $r_0$ | $r_0$ | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ |
| I | Step-In | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ |
| I | Step-out | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ |
| II | Read Sector | 1 | 0 | 0 | m | S | E | C | 0 | 1 | 0 | 0 | m | L | E | U | 0 |
| II | Write Sector | 1 | 0 | 1 | m | S | E | C | $a_0$ | 1 | 0 | 1 | m | L | E | U | $a_0$ |
| III | Read Address | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 | 1 | 1 | 0 | 0 | 0 | E | U | 0 |
| III | Read Track | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 | 1 | 1 | 1 | 0 | 0 | E | U | 0 |
| III | Write Track | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 | 1 | 1 | 1 | 1 | 0 | E | U | 0 |
| IV | Force Interrupt | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

**TABLE 2. FLAG SUMMARY**

| Command Type | Bit No(s) | | Description |
|---|---|---|---|
| I | 0, 1 | $r_1$ $r_0$ = Stepping Motor Rate See Table 3 for Rate Summary | |
| I | 2 | V = Track Number Verify Flag | V = 0,No verify<br>V = 1,Verify on destination track |
| I | 3 | h = Head Load Flag | h = 0,Unload head at beginning<br>h = 1,Load head at beginning |
| I | 4 | T = Track Update Flag | T = 0,No update<br>T = 1,Update track register |
| II & III | 0 | $a_0$ = Data Address Mark | $a_0$ = 0,FB(DAM)<br>$a_0$ = 1,F8(deleted DAM) |
| II | 1 | C = Side Compare Flag | C = 0,Disable side compare<br>C = 1,Enable side compare |
| II & III | 1 | U = Update SSO | U = 0,Update SSO to 0<br>U = 1,Update SSO to 1 |
| II & III | 2 | E = 15 MS Delay | E = 0,No. 15 MS delay<br>E = 1,15 MS delay (30 MS for 1 Mhz) |
| II | 3 | S = Side Compare Flag | S = 0,Compare for side 0<br>S = 1,Compare for side 1 |
| II | 3 | L = Sector Length Flag | LSB's Sector Length in ID Field: L = 0: 00 256, 01 512, 10 1024, 11 128; L = 1: 00 128, 01 256, 10 512, 11 1024 |
| II | 4 | m = Multiple Record Flag | m = 0,Single record<br>m = 1,Multiple records |
| IV | 0-3 | $I_x$ = Interrupt Condition Flags<br>$I_0$ = 1 Not Ready To Ready Transition<br>$I_1$ = 1 Ready To Not Ready Transition<br>$I_2$ = 1 Index Pulse<br>$I_3$ = 1 Immediate Interrupt, Requires A Reset*<br>$I_3$-$I_0$ = 0 Terminate With No Interrupt (INTRQ) | |

NOTE: See Type IV Command Description for further information.

**WRITE PRECOMPENSATION**

When operating in Double Density mode ($\overline{DDEN} = 0$), the WD279X has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST} = 0$.

**DATA SEPARATION**

The WD279X can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To program the 279X for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST} = 0$. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8" Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation.

Note: To maintain this mode, $\overline{TEST}$ must be held low whenever MR is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG 43), adjust the RPW pulse (250 ns for 8" Double Density). An external variable capacitor of C-60 pf is tied to the VCO input (Pin 26). It is highly recommended to use at least a negative 3500 PPM Temperature coefficient trimmer capacitor. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8" Double Density). The DDEN line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

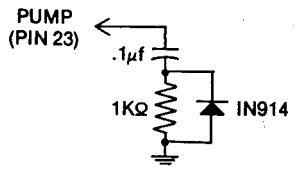
After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, which their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCP to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP runaway. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:




Since 5¼" Drives operate at exactly one-half the data rate (250 Kb/sec) the above capacitor should be doubled to .2 or .22 μf.

NOTE 1: A Diode with the lowest on resistance will enhance PUMP response.

NOTE 2: It is recommended to replace the 1K resistor with a 1K (nominal at 25°c) thermister (approximating 400 ohms at 50°c and approximatley 2.8K ohms at 0°c) to improve capture range.

**TYPE I COMMANDS**

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out commands. Each of the Type I Commands contains a rate field ($r_0$ $r_1$), which determines the stepping motor rate as defined in Table 3.

A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The direction signal is active high when stepping in and low when stepping out. The direction signal is valid before the first stepping pulse is generated. The rates (shown in Table 3) can be applied to a Step-Direction Motor through the device interface.

**TABLE 3. STEPPING RATES**

| CLK | | 2 MHz | 1 MHz |
|---|---|---|---|
| R1 | R0 | TEST = 1 | TEST = 1 |
| 0 | 0 | 3 ms | 6 ms |
| 0 | 1 | 6 ms | 12 ms |
| 1 | 0 | 10 ms | 20 ms |
| 1 | 1 | 15 ms | 30 ms |

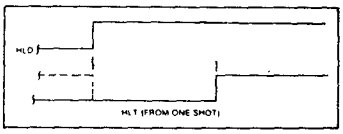
After the last directional step, an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

When a Seek, Step, or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation.

The WD279X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the WD279X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the WD279X which is used for the head engage time. When HLT = 1, the WD279X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the WD279X.




**HEAD LOAD TIMING**

When both HLD and HLT are true, the WD279X will then read from or write to the media. The "and" of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the WD279X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the WD279X then waits for HLT to occur.

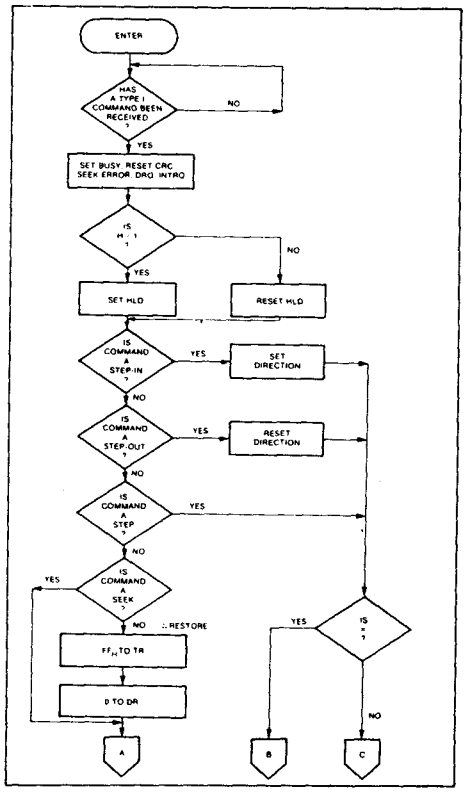
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

**RESTORE (SEEK TRACK 0)**

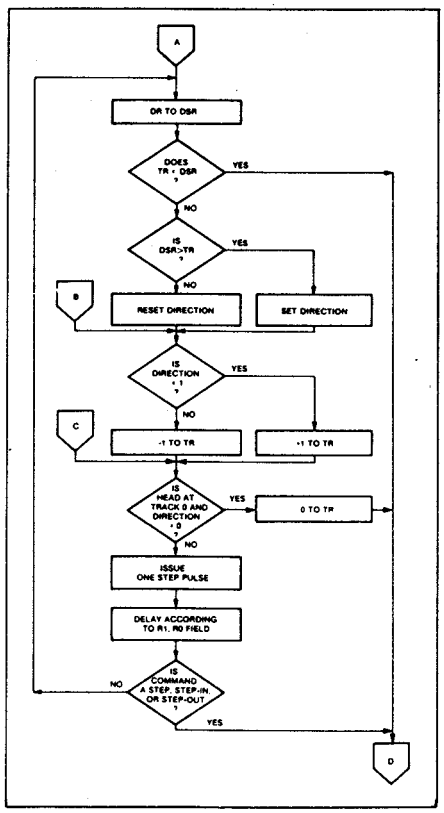
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read- Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the WD279X terminates operation, interrupts, and sets the Seek error status bit. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

**SEEK**

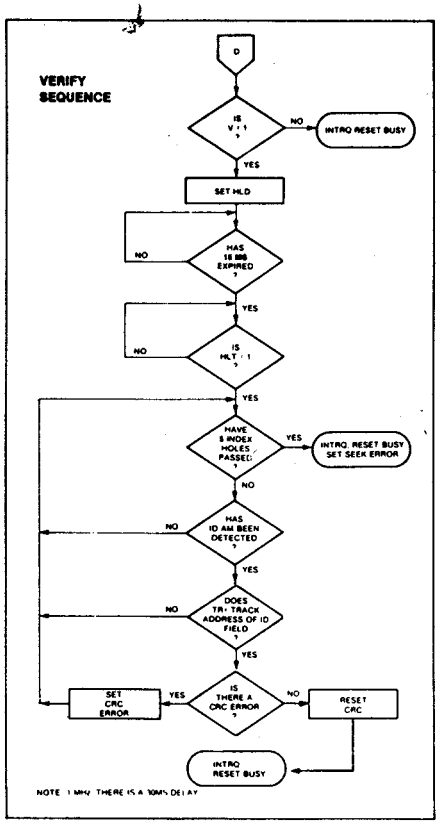
This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the




**TYPE I COMMAND FLOW**




TYPE I COMMAND FLOW




TYPE I COMMAND FLOW

appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

**STEP**

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command.

An interrupt is generated at the completion of the command.

**STEP-IN**

Upon receipt of this command, the WD279X issues one stepping pulse in the direction away from track zero. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**STEP-OUT**

Upon receipt of this command, the WD279X issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a

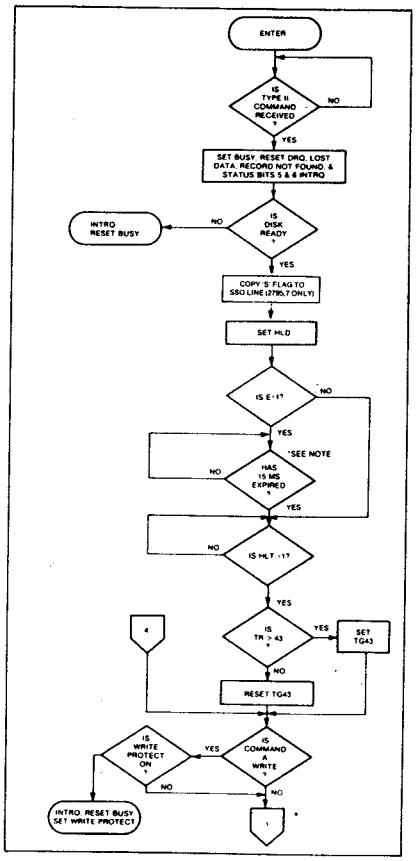
verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**EXCEPTIONS**

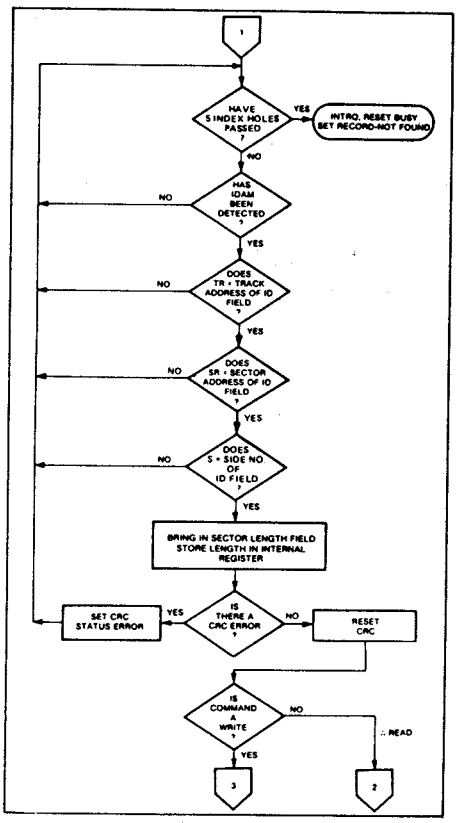
On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

**TYPE II COMMANDS**

The Type II Commands are the Read Sector and Write Sector commands. Prior to loadng the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay.



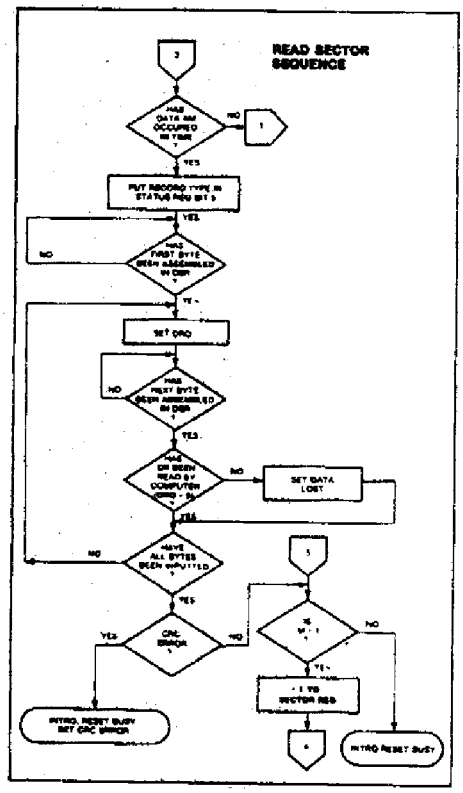

**TYPE II COMMAND**

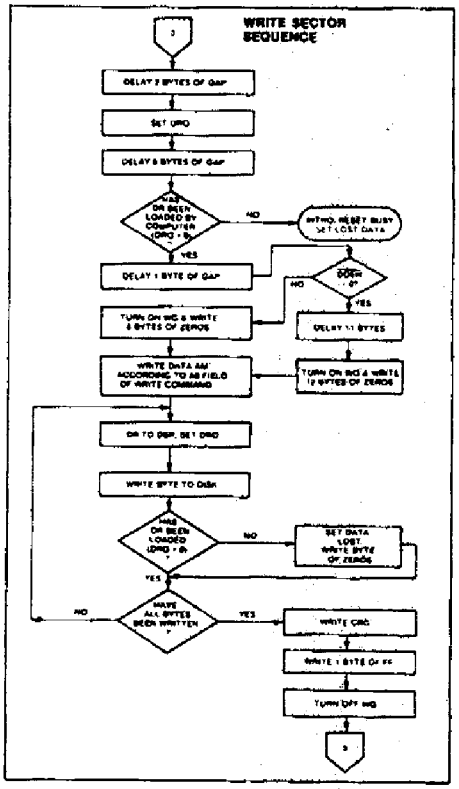



**TYPE II COMMAND**

When an ID field is located on the disk, the WD279X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is ready and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The WD279X must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command.




**TYPE II COMMAND**

If m = 1, multiple records are read or written with sector register internally updated so that an address verification can occur on the next record. The WD279X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD279X is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The WD279X will search for 5 disk revolutions, interrupt out, reset busy, and set the Record Not Found status bit.

The Type II commands for WD2791-93 also contain side select compare flags. When C = 0 (Bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag (Bit 3). If the S flag compares with the side number recorded in the ID field,

**TYPE II COMMAND**

the WD279X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III for the WD2795-97 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The WD2795/7 READ SECTOR and WRITE SECTOR commands include a 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to one.

**READ SECTOR**

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID

ld is encountered that has the correct track number, orrect sector number, correct side number, and cor- ct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the ost Data Status Bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector ommand).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

| STATUS BIT 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

**WRITE SECTOR**

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The D279X counts off 11 bytes in single density and 22 ytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command terminated and the Lost Data status bit is set. If ne DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a0 field of the command as shown below:

| a0 | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The WD279X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ will set 8 to 12μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

**TYPE III COMMANDS**
**READ ADDRESS**

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDR | SECTOR LENGTH | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transferred to the computer, the WD279X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

**READ TRACK**

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered Index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is

included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag will be set.

The ID A.M., ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

Because these synchronization problems almost always occur in the Data Area, this command will not function as a Track Copy and should be used only as a Diagnostic Program to test the ability to read addresses.

**WRITE TRACK FORMATTING THE DISK**

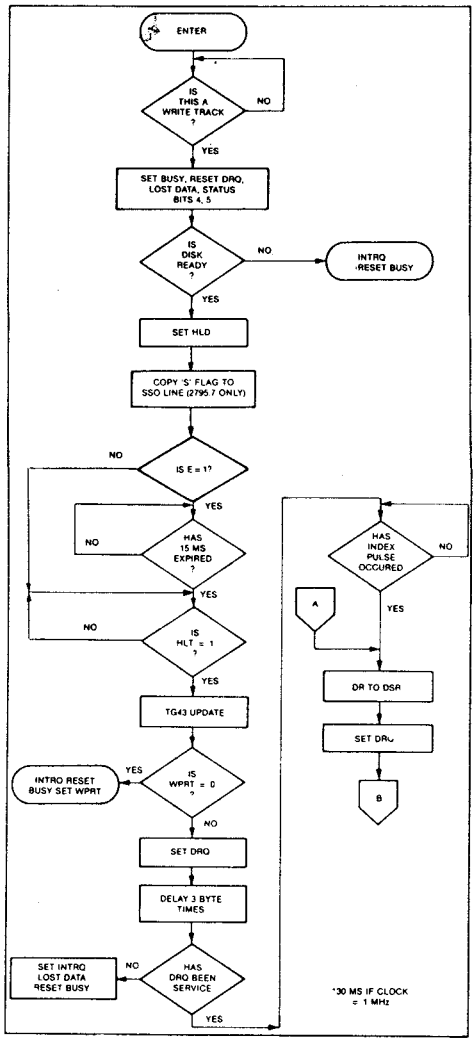
(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

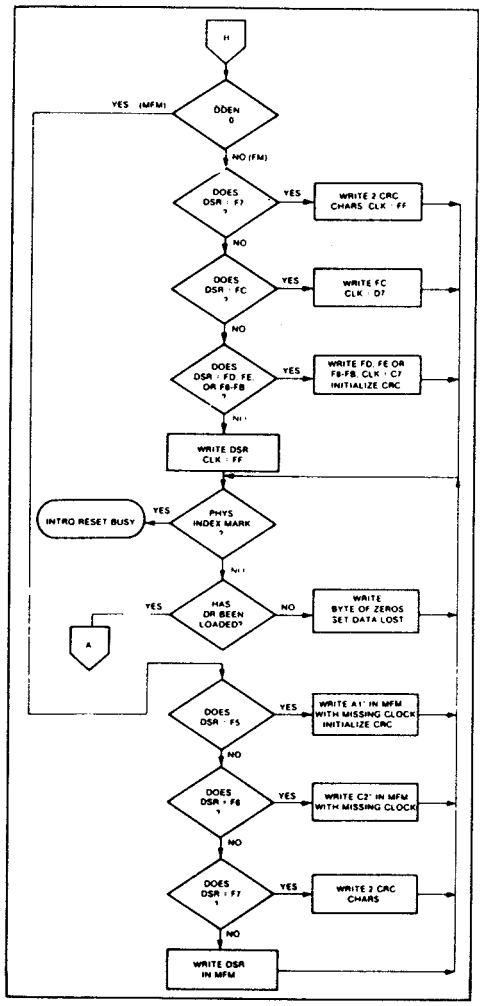
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by (within three byte times) the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, an the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the WD279X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM




**TYPE III COMMAND WRITE TRACK**




**TYPE III COMMAND WRITE TRACK**

**CONTROL BYTES FOR INITIALIZATION**

| DATA PATTERN IN DR (HEX) | WD279X INTERPRETATION IN FM (DDEN = 1) | WD279X INTERPRETATION IN MFM (DDEN = 0) |
|---|---|---|
| 00 thru F4 | Write 00 thru F4 with CLK = FF | Write 00 thru F4, in MFM |
| F5 | Not Allowed | Write A1* in MFM, Preset CRC |
| F6 | Not Allowed | Write C2** in MFM |
| F7 | Generate 2 CRC bytes | Generate 2 CRC bytes |
| F8 thru FB | Write F8 thru FB, CLK = C7, Preset CRC | Write F8 thru FB, in MFM |
| FC | Write FC with CLK = D7 | Write FC in MFM |
| FD | Write FD with CLK = FF | Write FD in MFM |
| FE | Write FE, CLK = C7, Preset CRC | Write FE in MFM |
| FF | Write FF with CLK = FF | Write FF in MFM |

*Missing clock transition between bits 4 and 5.

**Missing clock transition between bits 3 and 4.

or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

**TYPE IV COMMANDS**

The Forced Interrupt command is generally used to terminate a multiple sector Read or Write Command or to insure Type I status in the Status Register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

$I_0$ = Not-Ready to Ready Transition
$I_1$ = Ready to Not-Read Transition
$I_2$ = Every Index Pulse
$I_3$ = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3$-$I_0$) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If $I_3$-$I_0$ are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition ($I_3$ = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt.

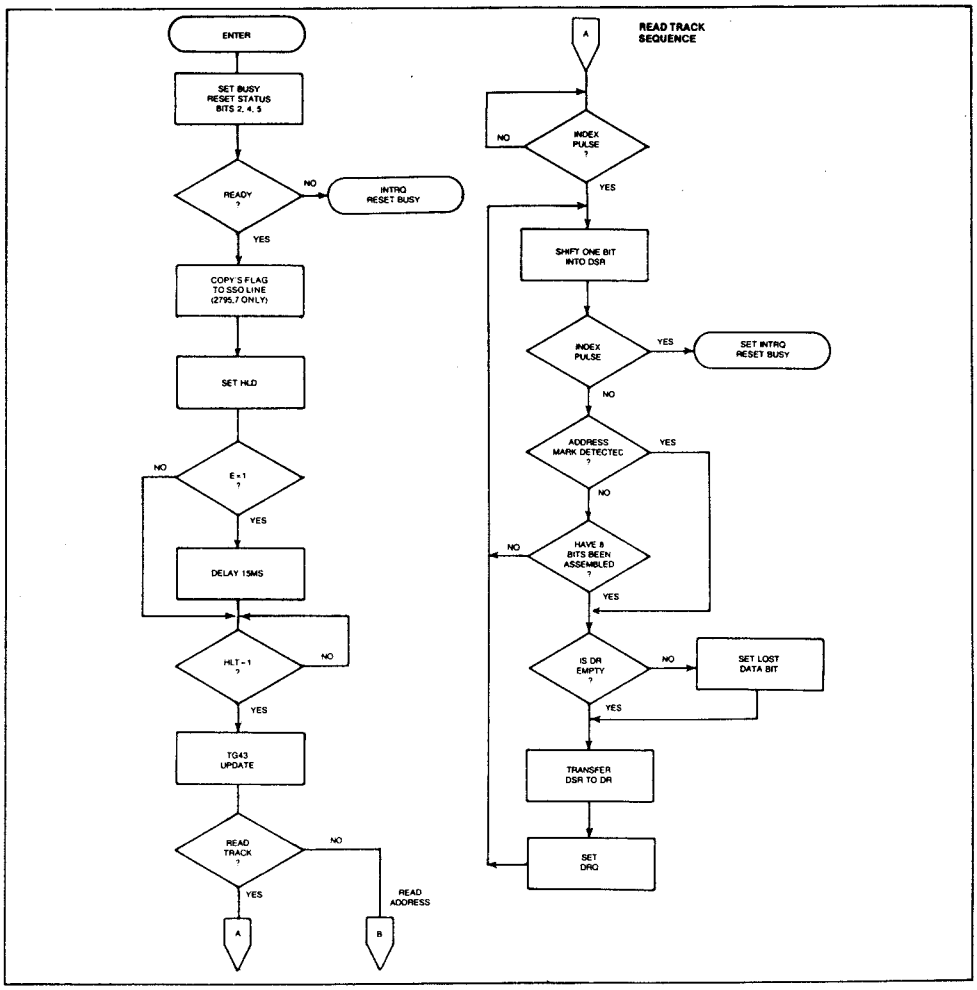
Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.).

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition ($I_1$ = 1) and the Every Index Pulse ($I_2$ = 1) are both set, the resultant command would be HEX "DA." The "OR" function is performed so that either a READY TO NOT-READY or the next Index Impulse will cause an interrupt condition.

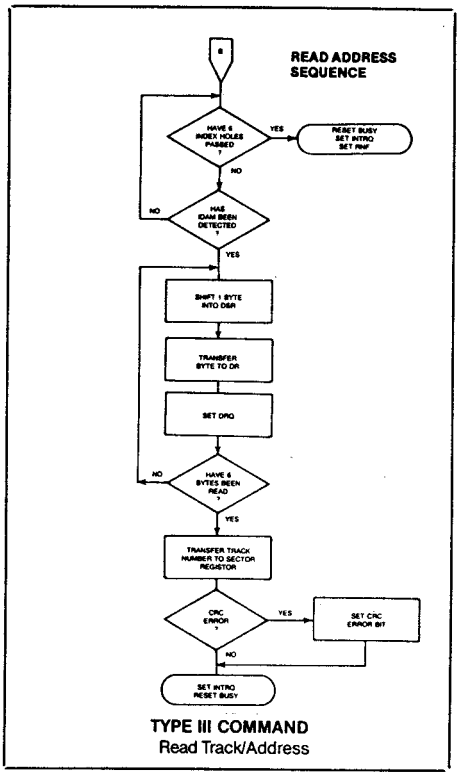
**STATUS REGISTER**

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register




**TYPE III COMMAND**
Read Track/Address




**TYPE III COMMAND**
Read Track/Address

is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

Status varies according to the type of command executed as shown in Table 4.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1 MHz)

| Operation | Next Operation | Delay Req'd. FM | MFM |
|---|---|---|---|
| Write to Command Reg. | Read Busy Bit (Status Bit 0) | 12μs | 6μs |
| Write to Command Reg. | Read Status Bits 1-7 | 28μs | 14μs |
| Write Any Register | Read From Diff. Register | 0 | 0 |

**IBM 3740 FORMAT - 128 BYTES/SECTOR**

Shown below is the IBM single density-format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track Command, and load the Data Register with the following values. For every byte to be written, there is one Data Request.

| NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|---|---|
| 40 | FF (or 00)[3] |
| 6 | 00 |
| 1 | FC (Index Mark) |
| [1]26 | FF (or 00) |
| 6 | 00 |
| 1 | FE (ID Address Mark) |
| 1 | Track Number |
| 1 | Side Number (00 or 01) |
| 1 | Sector Number (1 thru 1A) |
| 1 | 00 (Sector Length) |
| 1 | F7 (2 CRC's written) |
| 11 | FF (or 00) |
| 6 | 00 |
| 1 | FB (Data Address Mark) |
| 128 | Data (IBM uses E5) |
| 1 | F7 (2 CRC's written) |
| 27 | FF (or 00) |
| 247[2] | FF (or 00) |

1. Write bracketed field 26 times.
2. Continue writing until 279X interrupts out. Approx. 247 bytes.
3. A '00' option is allowed.

**IBM SYSTEM 34 FORMAT**
**256 BYTES/SECTOR**

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track Command and load the Data Register with the following values. For every byte to be written, there is one Data Request.

| NUMBER OF BYTES | HEX VALUE OF BYTE WRITTEN |
|---|---|
| 80 | 4E |
| 12 | 00 |
| 3 | F6 (Writes C2) |
| 1 | FC (Index Mark) |
| *50 | 4E |
| 12 | 00 |
| 3 | F5 (Writes A1) |
| 1 | FE (ID Address Mark) |
| 1 | Track Number (0 thru 4C) |
| 1 | Side Number (0 or 1) |
| 1 | Sector Number (1 thru 1A) |
| 1 | 01 (Sector Length) |
| 1 | F7 (2 CRC's written) |
| 22 | 4E |
| 12 | 00 |
| 3 | F5 (Writes A1) |
| 1 | FB (Data Address Mark) |
| 256 | DATA |
| 1 | F7 (2 CRC's written) |
| 54 | 4E |
| 598** | 4E |

*Write bracketed field 26 times.
**Continue writing until 279X interrupts out. Approx. 598 bytes.

### 1. NON-IBM FORMATS

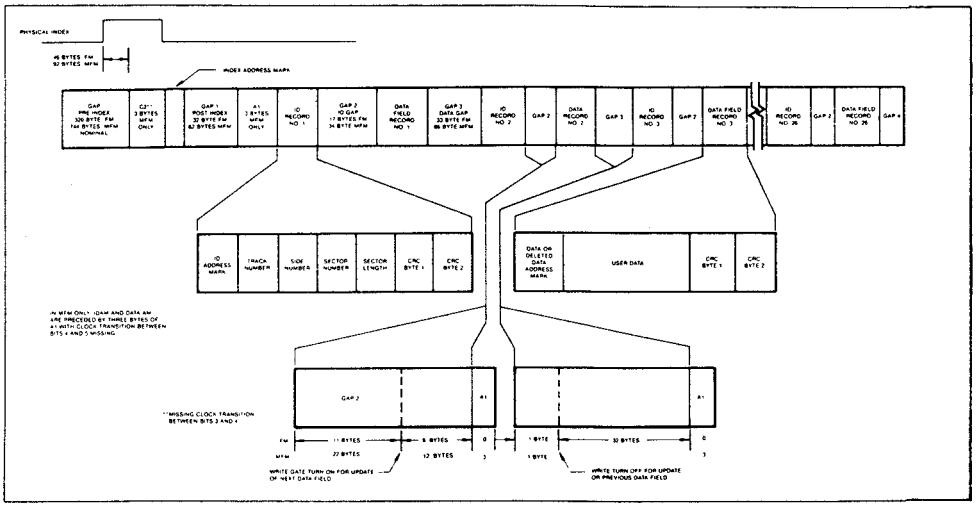
Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1. Sector size must be 128, 256, 512, of 1024 bytes.
2. Gap 2 cannot be vaired from the IBM format.
3. 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD279X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for WD279X operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

| | FM | MFM |
|---|---|---|
| Gap I | 16 bytes FF | 32 bytes 4E |
| Gap II | 11 bytes FF | 22 bytes 4E |
| * | 6 bytes 00 | 12 bytes 00 |
| * | | 3 bytes A1 |
| Gap III** | 10 bytes FF | 24 bytes 4E |
| | 4 bytes 00 | 8 bytes 00 |
| | | 3 bytes A1 |
| Gap IV | 16 bytes FF | 16 bytes 4E |

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.



IBM TRACK FORMAT

**ELECTRICAL CHARACTERISTICS**

Absolute Maximum Ratings

Voltage to any input with respect to $V_{SS}$ = +7 to -0.5V

Operating Temperature: +15°C to +50°C (NPO Capacitor, Pin 26)
+5°C to +60°C (minimum, Neg. 3500 TC capacitor, Pin 26)
0°C to +70°C (minimum, Neg. 3500 TC capacitor, Pin 26 and a thermistor in pump circuit)

Storage temperature = -55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating characteristics.

**OPERATING CHARACTERISTICS (DC)**

$T_A$ = See Electrical Characteristics

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage | | | 10 | µA | $V_{IN} = V_{CC}$ |
| $I_{OL}$ | Output Leakage | | | 10 | µA | $V_{OUT} = V_{CC}$ |
| $V_{IH}$ | Input High Voltage | 2.0 | | | V | |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_O$ = -100µA |
| $V_{OL}$ | Output Low Voltage | | | 0.45 | V | $I_O$ = 1.6mA |
| $V_{OHP}$ | Output High PUMP | 2.2 | | | V | $I_{OP}$ = -1.0 mA |
| $V_{OLP}$ | Output Low PUMP | | | 0.2 | V | $I_{OP}$ = +1.0 mA |
| $P_D$ | Power Dissipation | | | .75 | W | All Outputs Open |
| $R_{PU}$ | Internal Pull-Up* | 100 | | 1700 | µA | $V_{IN}$ = 0V |
| $I_{CC}$ | Supply Current | | 70 | 150 | mA | All Outputs Open |

*Internal Pull-up resistors on PINS 1, 17, 19, 22, 36, 37 and 40. Also pin 25 on WD2791 and 3.

**TIMING CHARACTERISTICS**

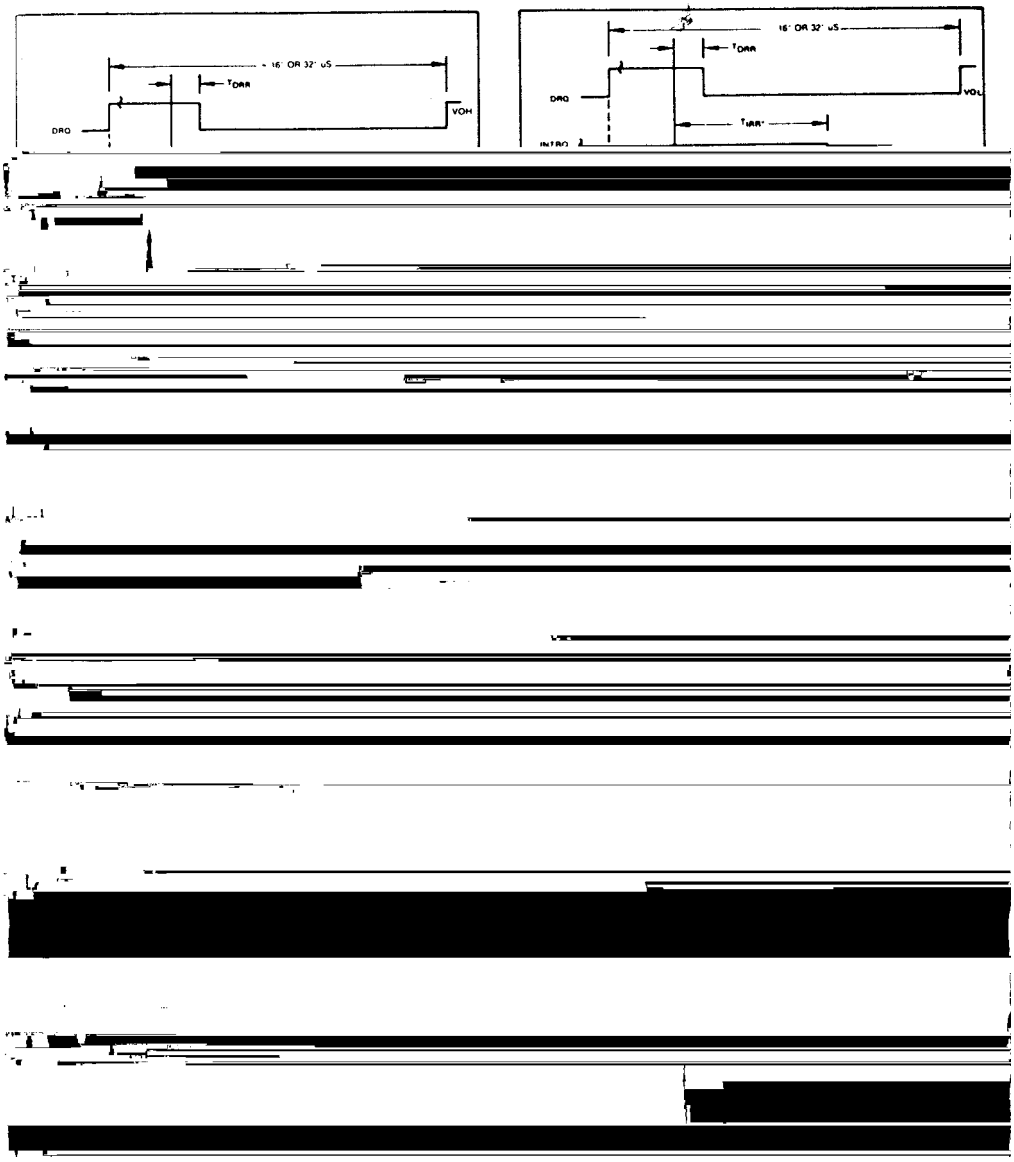
$T_A$ See Electrical Characteristics $V_{SS}$ = OV, $V_{CC}$ = +5 ±.25V

**READ ENABLE TIMING** (See Note 2.)

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $T_{SET}$ | Setup ADDR & CS to $\overline{RE}$ | 50 | | | nsec | See Note 3 |
| $T_{HLD}$ | Hold ADDR & CS from $\overline{RE}$ | 10 | | | nsec | |
| $T_{RE}$ | $\overline{RE}$ Pulse Width | 200 | | | nsec | $C_L$ = 50 pf |
| $T_{DRR}$ | DRQ Reset from $\overline{RE}$ | | 100 | 200 | nsec | |
| $T_{IRR}$ | INTRQ Reset from $\overline{RE}$ | | 500 | 3000 | nsec | See Fig. 3 |
| $T_{DACC}$ | Data Valid from $\overline{RE}$ | | 100 | 200 | nsec | $C_L$ = 50 pf |
| $T_{DOH}$ | Data Hold From $\overline{RE}$ | 20 | | 150 | nsec | $C_L$ = 50 pf |

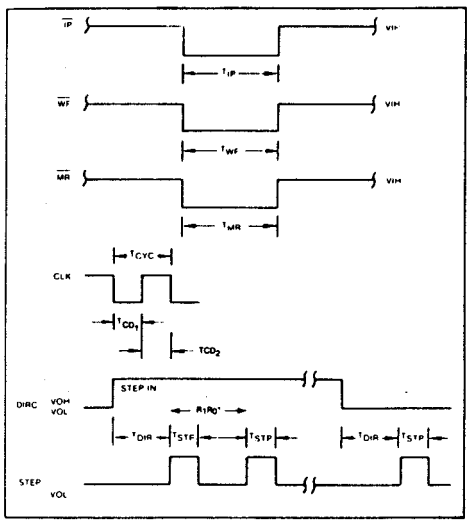
**WRITE ENABLE TIMING** (See Note 2)

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $T_{SET}$ | Setup ADDRS & CS TO $\overline{WE}$ | 50 | | | nsec | See Note 3 |
| $T_{HLD}$ | Hold ADDR & CS from $\overline{WE}$ | 10 | | | nsec | |
| $T_{WE}$ | $\overline{WE}$ Pulse Width | 200 | | | nsec | |
| $T_{DRR}$ | DRQ Reset from $\overline{WE}$ | | 100 | 200 | nsec | |
| $T_{IRR}$ | INTRQ Reset from $\overline{WE}$ | | 500 | 3000 | nsec | See Fig. 4 |
| $T_{DS}$ | Data Setup to $\overline{WE}$ | 150 | | | nsec | |
| $T_{DH}$ | Data Hold from $\overline{WE}$ | 50 | | | nsec | |


16 OR 32 uS
TDRR
DRQ
VOH
16 OR 32 uS
TDRR
DRQ
VOL
TMRT
INTRQ

**MISCELLANEOUS TIMING:**

| SYMBOL | CHARACTERISTIC | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| $T_{CD1}$ | Clock Duty (low) | 230 | 250 | 20000 | nsec | |
| $T_{CD2}$ | Clock Duty (high) | 230 | 250 | 20000 | nsec | |
| $T_{STP}$ | Step Pulse Output | 2 or 4 | | | µsec | See Notes 1 & 2 |
| $T_{DIR}$ | Dir Setup to Step | | 12 | | µsec | ± CLK ERROR |
| $T_{MR}$ | Master Reset Pulse Width | 50 | | | µsec | |
| $T_{IP}$ | Index Pulse Width | 10 | | | µsec | See Notes 1 & 2 |
| RPW | Read Window Pulse Width | | | | | Input 0-5V |
| | | 120 | | 700 | nsec | MFM |
| | | 240 | | 1400 | nsec | FM ± 15% |
| | Precomp. Adjust | 100 | | 300 | nsec | MFM |
| WPW | Write Data Pulse Width | | | | | Precomp = 100 nsec |
| | | 200 | 300 | 400 | nsec | MFM |
| WPW | Write Data Pulse Width | | | | | Precomp = 300 nsec |
| | | 600 | 900 | 1200 | nsec | MFM |
| VCO | Free Run Voltage Controlled | 6.0 | | | MHz | Cext = 0 |
| | Oscillator. Adjustable by ext. capacitor on Pin 26 | | 4.0 | | MHz | Cext = 35 pf |
| | Pump Up +25% | 5.0 | | | MHz | PU = 2.2V Cext = 35 pf |
| VCO | Pump Down -25% | | | 3.0 | MHz | $\overline{PD}$ = 0.2V Cext = 35 pf |
| | 5% Change $V_{CC}$ | 3.8 | | 4.2 | MHz | Cext = 35 pf |
| VCO | $T_A$ = 75°C | 3.5 | | | MHz | Cext = 35 pf |
| Cext | Adjustable external capacitor | 6 | 25 | 60 | pf | VCO = 4.0 MHz nom |
| RCLK | Derived read clock = VCO + 8, 16, 32 | | | | | VCO = 4.0 MHz |
| | | | 500 | | KHz | $\overline{DDEN}$ = 0 $\overline{5/8}$ = 1 |
| | | | 250 | | KHz | $\overline{DDEN}$ = 0 $\overline{5/8}$ = 0 |
| | | | 250 | | KHz | $\overline{DDEN}$ = 1 $\overline{5/8}$ = 1 |
| | | | 125 | | KHz | $\overline{DDEN}$ = 1 $\overline{5/8}$ = 0 |
| PU/DON | PU/$\overline{PD}$ time on (pulse width) | | | 250 | ns | MFM |
| | | | | 500 | ns | FM |

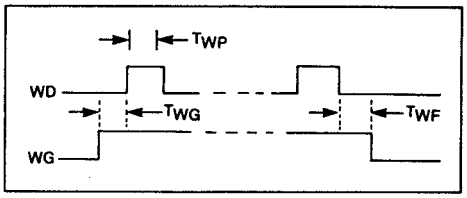



MISCELLANEOUS TIMING

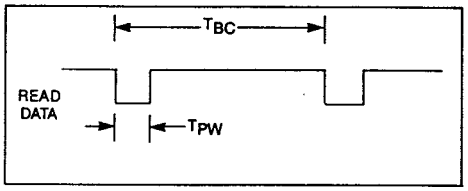
*FROM STEP RATE TABLE

**NOTES:**

1. Times double when clock = 1 MHz.
2. Output timing readings are at $V_{OL}$ = 0.8v and $V_{OH}$ = 2.0v.
3. $T_{SET}$ may be reduced to 0 nsec if $T_{RE}$ and $T_{WE}$ are increased the same amount.




WRITE DATA TIMING




READ DATA TIMING

**Table 4. STATUS REGISTER SUMMARY**

| BIT | ALL TYPE I COMMANDS | READ ADDRESS | READ SECTOR | READ TRACK | WRITE SECTOR | WRITE TRACK |
|---|---|---|---|---|---|---|
| S7 | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY | NOT READY |
| S6 | WRITE PROTECT | 0 | 0 | 0 | WRITE PROTECT | WRITE PROTECT |
| S5 | HEAD LOADED | 0 | RECORD TYPE | 0 | 0 | 0 |
| S4 | SEEK ERROR | RNF | RNF | 0 | RNF | 0 |
| S3 | CRC ERROR | CRC ERROR | CRC ERROR | 0 | CRC ERROR | 0 |
| S2 | TRACK 0 | LOST DATA | LOST DATA | LOST DATA | LOST DATA | LOST DATA |
| S1 | INDEX PULSE | DRQ | DRQ | DRQ | DRQ | DRQ |
| S0 | BUSY | BUSY | BUSY | BUSY | BUSY | BUSY |

**STATUS FOR TYPE I COMMANDS**

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ORed" with MR. |
| S6 PROTECTED | When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input. |
| S5 HEAD LOADED | When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals. |
| S4 SEEK ERROR | When set, the desired track was not verified. This bit is reset to 0 when updated. |
| S3 CRC ERROR | CRC encountered in ID field. |
| S2 TRACK 00 | When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input. |
| S1 INDEX | When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input. |
| S0 BUSY | When set command is in progress. When reset no command is in progress. |

**STATUS FOR TYPE II AND III COMMANDS**

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready. |
| S6 WRITE PROTECT | On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated. |
| S5 RECORD TYPE | On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a zero. |
| S4 RECORD NOT FOUND (RNF) | When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated. |
| S3 CRC ERROR | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated. |
| S2 LOST DATA | When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 DATA REQUEST | This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. |
| S0 BUSY | When set, command is under execution. When reset, no command is under execution. |

**SUMMARY OF ADJUSTMENT PROCEDURE**

**WRITE PRECOMPENSATION**

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe MR (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

**DATA SEPARATOR**

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe MR (Pin 19). Insure that 5 /8, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for (205ns for 8" DD 450ns for 5 1/4" DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500 KHz for 8" DD, 250 KHz for 5 1/4" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

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# WD279X-02 Floppy Disk Formatter/Controller Family Application Notes



## INTRODUCTION

In an effort to simplify Floppy Diskette interfacing, Western Digital has been constantly improving the LSI Controller/Formatter, the most recent of which is the WD279X Family of LSI controller devices, incorporating advanced technology to include controller, Write Compensation and Analog Phase Lock Loop in a single 40-pin dual-in-line package. With this package we can now offer the designer the simplest ever interfacing option.

The family consists of four members: WD2791, WD2793, WD2795 and WD2797. WD2791 and WD2793 offer internal clock divide in true and inverted data bus. The WD2795 and WD2797 offer internal side select. The family supports both 5 1/4" and 8" Diskette Drives and both single and double density.

## HOST INTERFACING

The LSI Diskette Controller has been developed to ease the interfacing of Processor to Disk Device. The Host interfacing with WD279X Family is accomplished with minimum external devices via an 8-bit bi-directional bus, read/write controls, register select lines and optional control line for chip select, 5 1/4" or 8" select, enable mini floppy, double density enable. The basic operation at the controller is accomplished by selecting the device via (CS) chip select line, enabling selection of one of the five internal registers (Figure 1).

| A1 - A0 | READ (RE) | WRITE (WE) |
|---|---|---|
| 0 0 | Status Regiser | Command Register |
| 0 1 | Track Register | Track Register |
| 1 0 | Sector Register | Sector Register |
| 1 1 | Data Register | Data Register |

FIGURE 1.

Each time a command is issued to the WD279X, the busy bit is set and INTRQ (Interrupt Request) line is reset. The user has the option of testing for the busy bit or polling INTRQ to determine if command has been completed.

The busy bit will be reset whenever the WD279X is idle and awaiting a new command. The INTRQ line once set, can only be reset by reading of the status register or issuing a new command.

The $A_0$, $A_1$ Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6250, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the WD279X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

| OPERATION | NEXT OPERATION | DELAY FM | REQ'D. MFM |
|---|---|---|---|
| Write to Command Reg. | Read Busy Bit (Status Bit 0) | 12μs | 6μs |
| Write to Command Reg. | Read Status Bits 1-7 | 28μs | 14μs |
| Write Any Register | Read From Diff. Register | 0 | 0 |

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2 MHz (8" drive) or 1 MHz (5 1/4" drive) with 50% duty cycle. Accuracy should be +1% (crystal source) since all internal timing, including stepping rates, are based upon this clock, or a single 2 MHz CLK on WD2791 and WD2793 since $\overline{ENMF}$ line will internally divide CLK.

The Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The WD179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TR00}$ line to go active low. This line should be connected to the drive's $\overline{TR00}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

The 5/8 Line selects internal VCO frequency to be used with 5 1/4" or 8" drives.

## FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection

to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs rom the WD279X. Inputs to the WD279X may be buffered or tied to the Drives' outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed -0.3 volts, while integrity of $V_{IH}$ and $V_{OH}$ levels should be kept within spec.

**MOTOR CONTROL**

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. sensor that informs the WD279X that the stepper motor is at is furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open," Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The WD279X will look at the ready signal prior to executing READ/WRITE commands. READY is not inspected during any Type 1 commands. All Type 1 commands will execute regardless of the Logic Level on this Line.

**GENERAL DISK WRITE OPERATION**

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the WD279X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set.

**RESTORE (SEEK TRACK 0)**

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the $r_1$ $r_0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the WD279X terminates operations, interrupts, and sets the Seek error status bit. A verification operation also takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

**SEEK**

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD279X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

**STEP**

Upon receipt of this command, the WD279X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**STEP-IN**

Upon receipt of this command, the WD279X issues one stepping pulse in the direction away from track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the $r_1$ $r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**EXCEPTIONS**

On the WD2795/7 devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

For write operations, the WD279X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

**READY**

Whenever a Read or Write command (Type II or III) is received the WD279X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

**COMMAND DESCRIPTION**

The WD279X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, and interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1 and Table 2.

**TABLE 1. COMMAND SUMMARY**

A. Commands for Models: 2791, 2793

| | Bits | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Type Command | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I Restore | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| I Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| I Step | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ |
| I Step-in | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ |
| I Step-out | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ |
| II Read Sector | 1 | 0 | 0 | m | S | E | C | 0 |
| II Write Sector | 1 | 0 | 1 | m | S | E | C | $a_0$ |
| III Read Address | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 |
| III Read Track | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 |
| III Write Track | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 |
| IV Force Interrupt | 1 | 1 | 0 | $I_1$ | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

B. Commands for Models: 2795, 2797

| | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I Restore | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| I Seek | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| I Step | 0 | 0 | 1 | T | h | V | $r_1$ | $r_0$ |
| I Step-in | 0 | 1 | 0 | T | h | V | $r_1$ | $r_0$ |
| I Step-out | 0 | 1 | 1 | T | h | V | $r_1$ | $r_0$ |
| II Read Sector | 1 | 0 | 0 | m | L | E | U | 0 |
| II Write Sector | 1 | 0 | 1 | m | L | E | U | $a_0$ |
| III Read Address | 1 | 1 | 0 | 0 | 0 | E | U | 0 |
| III Read Track | 1 | 1 | 1 | 0 | 0 | E | U | 0 |
| III Write Track | 1 | 1 | 1 | 1 | 0 | E | U | 0 |
| IV Force Interrupt | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

**TABLE 2. FLAG SUMMARY**

| Command Type | Bit No(s) | | Description |
|---|---|---|---|
| I | 0, 1 | $r_1$ $r_0$ = Stepping Motor Rate<br>See Table 3 for Rate Summary | |
| I | 2 | V = Track Number Verify Flag | V = 0,No verify<br>V = 1,Verify on destination track |
| I | 3 | h = Head Load Flag | h = 0,Load head at beginning<br>h = 2,Unload head at beginning |
| I | 4 | T = Track Update Flag | T = 0,No update<br>T = 1,Update track register |
| II | 0 | $a_0$ = Data Address Mark | $a_0$ = 0,FB(DAM)<br>$a_0$ = 1,F8(deleted DAM) |
| II & III | 1 | C = Side Compare Flag | C = 0,Disable side compare<br>C = 1,Enable side compare |
| II & III | 1 | U = Update SSO | U = 0,Update SSO to 0<br>U = 1,Update SSO to 1 |
| II & III | 2 | E = 15 MS Delay | E = 0,No 15 MS delay<br>E = 1,15 MS delay (30 MS for 1 MHz) |
| II | 3 | S = Side Compare Flag | S = 0,Compare for side 0<br>S = 1,Compare for side 1 |
| II | 3 | L = Sector Length Flag | |

| LSB's Sector Length in ID Field | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| L = 0 | 256 | 512 | 1024 | 128 |
| L = 1 | 128 | 256 | 512 | 1024 |

| | | | |
|---|---|---|---|
| II | 4 | m = Multiple Record Flag | m = 0,Single record<br>m = 1,Multiple records |
| IV | 0-3 | $I_x$ = Interrupt Condition Flags<br>$I_0$ = 1 Not Ready To Ready Transition<br>$I_1$ = 1 Ready To Not Ready Transition<br>$I_2$ = 1 Index Pulse<br>$I_3$ = 1 Immediate Interrupt, Requires A Reset*<br>$I_3$-$I_0$ = 0 Terminate With No Interrupt (INTRQ) | |

*NOTE: See Type IV Command Description for further information.